# Design of a 0.7~1.5 GHz Wideband Power Amplifier in 0.18-µm CMOS Process

# Xiangning Fan, Zhou Yu, Jiakai Lu, and Zaijun Hua

Institute of RF&OE-ICs, School of Information Science and Engineering Southeast University, Nanjing, 210096, China xnfan@seu.edu.cn

Abstract – A power amplifier (PA) for multi-mode multi-standard transceiver which is implemented in a TSMC 0.18-µm CMOS process is presented. The proposed PA improves bandwidth using matching compensation, lossy matching network and negative feedback technique. Measurement results show that the working frequency range of the wideband PA is 0.7~1.5GHz, with the maximum output power of 18.2~22.3dBm. The output P1dB during test is 16.6~21.4 dBm, and the corresponding power added efficiency (PAE) is 7.7%~23.4%. The power gain within the working frequency is larger than 16dB and the S11 is less than -13dB. According to the test results, the proposed PA can cover the frequency of more than one octave. The linearity and power gain of the PA is satisfactory within the working frequency.

*Index Terms* – CMOS power amplifiers, lossy matching network, wideband amplifier, wideband matching.

## **I. INTRODUCTION**

In the past decade, with the development of wireless communication technology, more and more modern wireless communication standards and applications emerged. An integrated multi-standard RF front-end which can cover GSM, LTE, WLAN, Bluetooth and GPS is required in this information era. Therefore, a fully integrated multi-mode multi-standard mobile front-end increasingly attracts the focus of industry and research [1].

However, conventional multi-mode transceivers are often implemented with some narrow band PAs for each frequency band [2], which increases the chip area and power cost. With the growing number of standards which the transceiver needs to support, wideband PAs draw more and more attention. Compared with narrow band Pas, wideband PAs have advantages of high integration and low cost.

Common methods of wideband matching network designing contain two major directions. Some wide band PAs are designed with tunable matching network of which the resonance frequency is tunable by switches [3], switched capacitors [4] or variable inductors. Another design method is a single wideband matching network which can directly cover the whole working bands [5].

Nowadays, most of RF PA is implemented in GaAs technology for its superior device performance [6]. However, CMOS process, which has the merit of high integration level and low cost, becomes a choice for designing PAs. In this work, a 0.7-1.5GHz CMOS power amplifier is designed in TSMC 0.18µm process.

The outline of this paper is as follows. Section II introduces the main techniques used in the design, i.e., wideband matching technology. Section III describes the circuit design of the proposed wideband PA. Measurement results are given in Section IV. Finally, summary of this work follows in Section V.

# **II. WIDEBAND MATCHING TECHNOLOGY**

To ensure a good performance over whole frequency range of 0.7~1.5GHz, the power amplifier should have wideband matching network features.

In common structures of multi-mode power amplifier, wideband design and multi-band combination are two major design directions. Conventional multimode transceivers are often implemented with some narrow band PAs for each frequency band, which increases the chip area and power cost.

With the growing number of communication standards, wideband design becomes more attractive. Some wideband PAs are designed with tunable matching network of which the resonance frequency is tunable by switches, switched capacitors or variable inductors. Another design method is a single wideband matching network which can directly cover the whole working bands.

The wideband matching technique mainly adopts in this design include matching compensation technique, lossy matching network and negative feedback.

### A. Matching compensation technique

Parasitic capacitances of MOS tube result in gain of power transistor rolls off at a rate of 6dB per octave.

Matching compensation technique is often applied for matching the output impedance of driver stage and the input impedance of power stage at the high frequency band. The mismatch at low frequency results in gain attenuation. Therefore, the flat gain across the whole frequency range can be expected, as shown in Fig. 1.

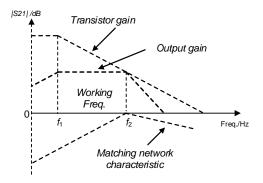


Fig. 1. Matching compensation of inter-stage network.

#### **B.** Lossy matching network

Lossy matching structure is shown in Fig. 2. Similar to mathing compensation technique, lossy mathing network attenuates the low-frequency gain by introducing resistance. In Fig. 2 (a), in the low frequency range, the inductor can be seen as a short circuit, and signal flows to the ground through the resistor, which absorbs low frequency energy. While in the high frequency range, the impedance of the inductor is so large that signal cannot pass through. In Fig. 2 (b), in the low frequency range, the capacitor branch can be seen as open, and signal flows through the resistor. Thus, these matching networks can adjust the low frequency gain and improve the bandwidth.

When designing wideband PA, the impedance may change rapidly in a wide frequency range. By adding resistor, the input matching can be realized easily. But for maximum output power, the resistors cannot be used in output matching network.

Furthermore, it can greatly improve the stability of the amplifier. Though it increases the noise factor of amplifier, it is still widely used in wideband matching for PA.

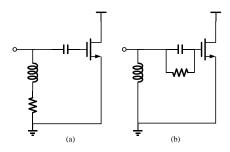


Fig. 2. Lossy matching network.

#### C. Negative feedback

The bandwidth of amplifier is restricted to the gain bandwidth product (GBW). Negative feedback is suitable for designing wideband amplifier which calls for flat gain performance. It can also improve the linearity of amplifier [7] and simplify the design of matching network.

Considering the power stage in Fig. 3. The resistor  $R_f$  is designed to adjust the gain of transistor, and the capacitor  $C_f$  blocks DC signal. When there is no feedback path on the transistor, the output power is expressed by:

$$P_{O} = V_{o}^{2} / R_{L} = (g_{m}V_{1})^{2} R_{L}.$$
 (1)

With the RC feedback path, the output power is changed to  $P_{ofb}$ , which can be expressed by:

$$P_{ofb} = V_o^2 / R_L = (g_m V_1)^2 R_L g (\frac{1 - 1/g_m R_f}{1 + R_L / R_f})^2.$$
(2)

Therefore, the power loss caused by the negative feedback can be expressed by:

$$\frac{P_{ofb}}{P_o} = \left(\frac{1 - 1/g_m R_f}{1 + R_L/R_f}\right)^2.$$
 (3)

When  $R_f >> R_L$ , the power loss can be expressed by:

$$\frac{P_{ofb}}{P_o} \approx 1 - \frac{2R_L}{R_f}.$$
(4)

As shown in (4), the feedback resistor  $R_f$  will cause the power loss  $\rho f$  the PA. Negative feedback can also influence the stability of amplifier [1].

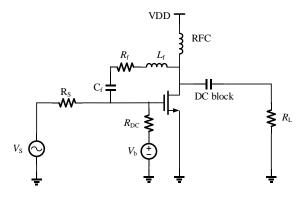


Fig. 3. Feedback amplifier structure.

#### **D.** Low-Q multi-stage matching network

Usually, simple single stage lumped components matching network cannot reach large bandwidth impedance transformation and is only used in the narrow-band matching. The output matching network is realized by low Q multi-stage impedance matching network, as shown in Fig. 5. The Q value, working bandwidth and center frequency can be expressed as:

$$Q = f_0 / BW.$$
 (5)

Maximum Q factor of network is:

$$Q_{\rm max} = \sqrt{f_H \times f_L} / BW. \tag{6}$$

For wideband power amplifier, the impedance conversion ratio between the optimum impedance and the 50 $\Omega$  port impedance is very large, which means a long distance between two impedance points on Smith chart. The Q factor of the network will limit the values of matching components.

Figure 4 (a) shows the scheme of using a single L type matching network, while Fig. 4 (b) using a multistage L type matching network. Apparently, by using multi-stage L type matching network, the Q factor can be smaller and the band extended.  $R_1$  and  $R_2$  are virtual resistances for matching, their values are between  $R_s$  and  $R_L$ . For n-stage L type matching network, assume  $R_s>R_L$ , when the ratio of the adjacent resistors is equal, the optimal bandwidth can be achieved [8]:

$$\frac{R_{\rm s}}{R_{\rm l}} = \frac{R_{\rm l}}{R_{\rm 2}} = \dots = \frac{R_{\rm n-l}}{R_{\rm L}},\tag{7}$$

$$R_{1} = (R_{1}R_{3})^{1/2}$$

$$R_{2} = (R_{1}R_{3})^{1/2}$$
(8)

$$R_{n-1} = (R_{n-2}R_{\rm L})^{1/2}.$$

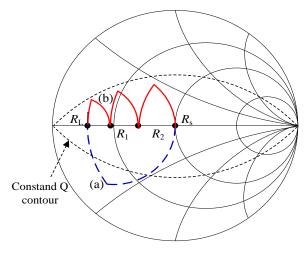


Fig. 4. Smith chart impedance transformation: (a) single L type matching network, and (b) multi-stage L type matching network.

### **III. WIDEBAND PA CIRCUIT DESIGN**

The proposed wideband PA is used for multi-mode multi-standard transceiver. It calls for the performance of PA on linearity, power gain and working frequency. Additionally, because the transceiver needs to handle non-constant envelop signal, the PA should be designed to work in linear regime.

As shown in Fig. 5 (a), the power amplifier employs a two-stage topology structure, i.e., the driver and output

stage, to have sufficient power gain. Both driver stage and output stage are biased as a Class-A amplifier to get maximum linearity. The driver stage is designed to provide high gain and the power stage should have sufficient power-handling capability.

Both input matching network and inter-stage matching network are realized with lossy network which introduces resistance element in the matching network. Resistance absorbs energy in low frequency range, thus the gain of low frequency and high frequency are equal.

The inter-stage matching network is designed to match the output impedance of driver stage and the input impedance of power stage at the high frequency band. The mismatch between the two impedances at low frequency range reduces the low frequency gain. Therefore, it can be expected that the flat gain across the whole frequency range, as shown in Fig. 5 (b).

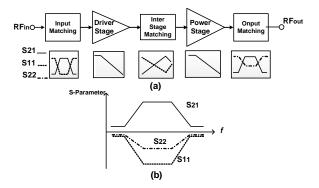


Fig. 5. Wideband power amplifier: (a) schematic diagram and (b) S-parameters.

All components outside of the dotted line frame in Fig. 6 are placed off-chip, including RF chokes and output matching network.  $L_{bond}$  is the equivalent inductance of bonding wire. The driver stage exploits a cascode structure to ensure sufficient gain. The cascode structure also improve the input-output isolation, thus simplified the design of matching network.

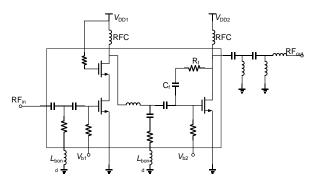


Fig. 6. Schematic diagram of two-stage wideband power amplifier.

TSMC 0.18 $\mu$ m CMOS process provides both thickoxide transistor and thin-oxide transistor. In the power stage, with the supply voltage of 3.3V, a thick-oxide transistor is used to sustain a large-voltage swing across the drain and the gate. The supply voltage of driver stage is 2V, so the devices in driver stage are both thin-oxide transistors.

The output matching network is realized by low Q multi-stage impedance matching network. Load-pull simulation results show that the optimum load impedance  $R_{opt}$  changes a little across working band. The low Q matching network transforms load impedance of 50 $\Omega$  close to  $R_{opt}$  over the working band so that the power stage has sufficient power-handling capability. The output impedance transformation is shown in Fig. 7. The real part of the impedance at the drain of output transistor is around 15 $\Omega$ , and the magnitude of the impedance is between 15 $\Omega$  and 20 $\Omega$ .

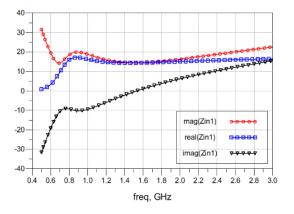


Fig. 7. Impedance transformation of output matching network.

Negative feedback technique is used in power stage to expand bandwidth of the amplifier. It is important to choose proper resistance that makes balance between power gain, bandwidth and stability.

#### **IV. MEASURENMENT RESULTS**

The proposed PA has been fabricated in TSMC 0.18 $\mu$ m process. The chip size of the PA is 0.98mm×0.46mm. Output matching network and RF choke inductors are off the chip. The photograph of the wideband PA is shown in Fig. 8.

According to the measurement results, the DC current of the driver stage and power stage are 32mA and 158mA, respectively. So the DC power consumption is about 585mW.

In the working band of 0.7~1.5GHz, the PA is set to be working at 9 frequency points. Figure 9 shows the measured output power of the PA at 700MHz. According to the relationship of input power and output power in Fig. 9, the power gain, 1dB compression points and efficiency can be calculated.

Figure 10 shows the measured power gain, maximum output power and S11 of the wideband PA. And Fig. 11 shows the measured output 1dB compression points and corresponding PAE (Power Added Efficiency).

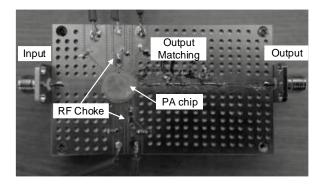


Fig. 8. Photograph of fabricated wideband PA.

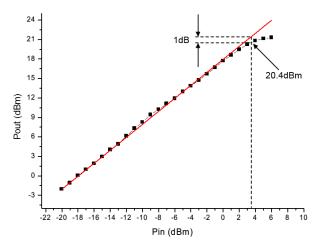


Fig. 9. Measured output power at 700MHz.

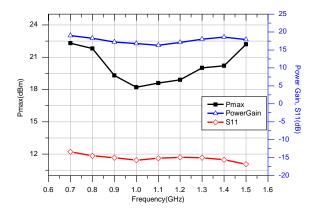


Fig. 10. Measured power gain, maximum output power and S11.

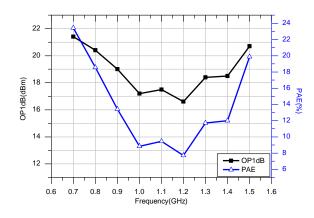


Fig. 11. Measured OP1dB and PAE @ OP1dB.

Within the frequency range of 0.7-1.5GHz, the PA can deliver maximum output power of more than 18dBm with the power gain between 16.3dB and 19dB. The small signal S-parameters of S11 is under -13dB across the frequency range. The OP1dBis between 16.6dBm and 21.4dBm and the PAE at OP1dB is 7.7%~23.4% through the working band. The overall performance of the designed PA with the recent state-of-the art results are summarized in Table 1.

Table 1: Summary of PA performance and comparison with proposed designs

| Ref.                       | [7]  | [8]   | [9]   | [10]    | This Work |
|----------------------------|------|-------|-------|---------|-----------|
| Freq.<br>(GHz)             | 6~10 | 3~7.5 | 0.5~5 | 0.9~3.0 | 0.7~1.5   |
| S11<br>(dB)                | <-8  | <-5   | <-15  | —       | <-13      |
| Gain<br>(dB)               | 8.5  | 10    | 10~15 | 12~17   | >16       |
| OP <sub>1dB</sub><br>(dBm) | 5    | >0    | 10~17 | 17~21   | 16.6~22   |
| Psat<br>(dBm)              | _    | >5    | 14~21 | 20~21   | 18.2~22   |
| PAE<br>(%)                 | 14.4 | 12    | 3~16  | 11~23   | 8~23.4    |
| CMOS<br>Tech (µm)          | 0.18 | 0.18  | 0.13  | 0.18    | 0.18      |

#### V. CONCLUSION

This work presents a wideband two-stage linear power amplifier operating from 0.7GHz to 1.5GHz. Lossy matching network, matching compensation and negative feedback are used to improve bandwidth. The measurement results show that the PA demonstrate the maximum output power of more than 18dBm with the power gain of 16.3~18dB within the working band. From 0.7GHz to 1.5GHz, the output 1dB compression point is more than 16.6dBm and can be above 21dBm at 700MHz. At the OP1dB, the PA can achieve 7.7%~23.4% power added efficiency. According to the test results, the proposed PA can cover the frequency of more than one octave with satisfactory power gain and linearity. This PA applies to multi-standard wireless communication applications, and can be used in multi-mode multistandard transceiver.

# ACKNOWLEDGMENT

This work is supported by the Priority Academic Program Development of Jiangsu Higher Education Institutions and Graduate Innovation Project of Jiangsu Province.

#### REFERENCES

- [1] S. S. Hyuk, Y. K. Woo, Y. J. Joo, et al., "A fully integrated CMOS class-E power amplifier for reconfigurable transmitters with WCDMA/WiMAX applications," *Proceedings of the 2013 26<sup>th</sup> International Conference on VLSI Design and* 2013 12<sup>th</sup> International Conference on Embedded Systems, pp. 169-172, 2013.
- [2] J. P. Young and N. Cheng, "Multimode multiband power amplifier optimization for mobile applications," *VLSI Technology, Systems, and Applications (VLSI-TSA)*, pp. 1,3, Apr. 2013.
- [3] K. Sungyoon, K. Unha, K. Youngwoo, et al., "A multi-mode multi-band reconfigurable power amplifier for low band GSM/UMTS handset applications," *Power Amplifiers for Wireless and Radio Applications (PAWR)*, pp. 16-18, Jan. 2013.
- [4] H. Wang, C. Sideris, and A. Hajimiri, "A CMOS wideband power amplifier with a transformerbased high-order output matching network," *IEEE Journal on Solid-State Circuits*, vol. 45, no. 12, pp. 2709-2722, Dec. 2010.
- [5] A. Grebennikov, *RF and Microwave Power Amplifier Design*. Publishing House of Electronics Industry, pp. 258-260, 2005.
- [6] A. Fukuda, T. Furuta, H. Okazaki, et al., "Low-loss matching network design for band-switchable multi-band power amplifier," *IEICE Transactions* on *Electronics*, vol. E95-C, pp. 1172-1181, July 2012.
- [7] H.-W. Chung, C.-Y. Hsu, C.-Y Yang, K.-F. Wei, and H.-R. Chuang, "A 6-10-GHz CMOS power amplifier with an inter-stage wideband impedance transformer for UWB transmitters," *Proceedings* of the 38<sup>th</sup> European Microwave Conference, pp. 305-308.
- [8] S. A. Z. Murad, R. K. Pokharel, H. Kanaya, and K. Yoshida, "A 3.0–7.5 GHz CMOS UWB PA for group 1~3 MB-OFDM application using current reused and shunt-shunt feedback," *The 2009 International Conference on Wireless Communication & Signal Processing*, pp. 1-4, 2009.
- [9] J. Roderick and H. Hashemi, "A 0.13µm CMOS

power amplifier with ultra-wide instantaneous bandwidth for imaging applications," *IEEE ISSCC Dig. Tech. Papers*, pp. 374-375, Feb. 2009.

[10] D. Imanishi, K. Okada, and A. Matsuzawa, "A 0.9-3.0 GHz fully integrated tunable CMOS power amplifier for multi-band transmitters," *IEEE Asian Solid-State Circuits Conference*, pp. 1-4, Nov. 16-18, 2009.



Xiangning Fan received the B.S. and M.S. degrees both from Nanjing University of Posts and Telecommunications in 1985 and 1988 respectively. From 1997, he becomes a part time Ph.D. in National Communications Research Laboratory (NCRL), Southeast

University and received the Ph.D. degree in 2005 with Grade A. Since 1988, he works in Southeast University and now he is a Full Professor in Institute of RF-&-OE-ICs, School of Information Science and Engineering, Southeast University. Fan has finished more than 20 national projects on WSN, UWB, and 3G/4G Mobile Systems, and published more than 130 papers in IEEE T-CAS, IEEE COMM. Letters, Signal Processing, IET Radar, Sonar & Navigation, Electronic Letters, Sensor Letters, Springer AICASP, etc. with about 100 papers SCI/Ei indexed. His current research interests include RF ICs, receiver design and signal processing of wireless systems.







**Zhou Yu** received the B.S. degree in Information Science and Engineering and the M.S. degree in Integrated Circuit Engineering at Southeast University, in 2012 and 2015. His present research interests include frequency transmitter and RF circuit design.

Jiakai Lu received the B.S. degree in Micro-electronics and the M.S. in integrated circuit engineering at Southeast University, in 2012 and 2015. His present research interests include RF integrated circuit design and transmitter design.

**Zaijun Hua** was born in Jiangyan, Jiangsu Province, in 1983. He received the B.S. and M.S. degrees in Telecommunication Engineering from Beijing Jiaotong University, Beijing, China, in 2006 and 2008, respectively, and is currently working toward the Ph.D. degree at

Southeast University. His research interests are RF transceivers.